Description

The NT8805C is a CMOS integrated circuit for use in transponders. The circuit is powered by an external coil placed in a magnetic field, and gets its clock from the same field via one of the coil terminals. The other coil terminal is affected by the modulator, turning on and off the modulation current in order to send back the 64 bits of information contained in a factory pre-programmed memory array.

The programming of the chip is performed by electrical fusing of polysilicon links in order to store a unique code on each chip.

The serial output data string contains a 9 bits header, 40 bits of data, 14 parity bits, and 1 stop bit.

Due to low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is required to obtain the chip function. A parallel capacitor adjusted with the coil to obtain resonance, will increase the read distance

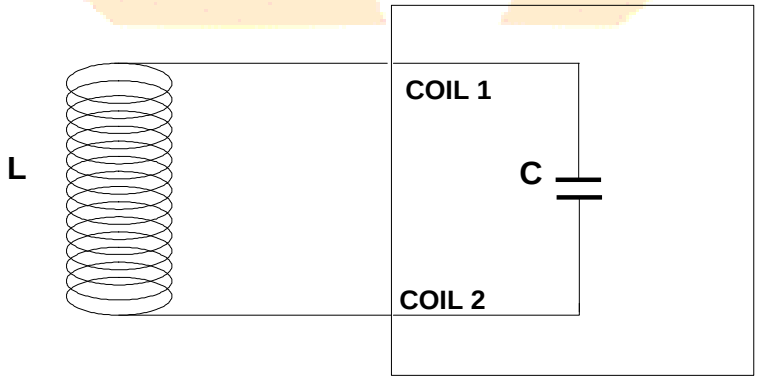
Features

- 64 bit memory array electrically programmable
- Wide dynamic range due to on chip buffer capacitance and voltage limiter on chip.
- Full wave rectifier on chip
- Big modulation depth due to a low impedance modulation device
- Very small chip size convenient for implantation
- Large distance even without resonance capacitor
- No external buffer capacitance needed due to low power consumption
- On chip resonant capacity

Application

- Industrial transponder
- Animal Transponder
- ID cards
- Serial Number Identification ROM

Typical Operating Configuration



Typical value of inductance at 125KHz is 3.52 mH
The capacitor is adjusted to the resonance

Absolute Maximum Ratings

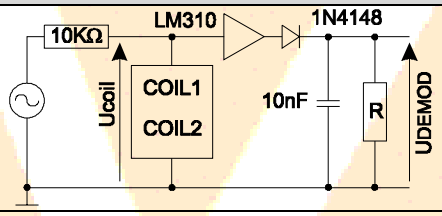
Parameter	Symbol	Conditions
Maximum AC peak current induced on COIL1 and COIL2	Icoil	30 mA
Maximum storage temperature	TSTMAX	+200°C
Minimum storage temperature	TSTMIN	-55°C

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40		+85	°C
AC Supply Voltage	Vcoil	3.5			Vpp
Supply Frequency	fcoil	100	125	150	KHz

Electrical Characteristics

Vcoil=3.5Vpp±5%, fcoil=125KHz Sine Wave, Topr=25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Demodulated Voltage	U_{DEMOD}		0.25			VAC
Dynamic Current	Idyn			50		μA
Build-in Capacitor	C			460		pF
Build-in Capacitor Tolerance					±5%	

Timing Characteristics

Vcoil1=3.5Vpp, Vcoil2=0V, Sine Wave

Parameter	Symbol	Min	Typ	Max	Unit
Coil Clock Frequency	fcoil	100	125	150	KHz
Ratio between coil period and bit period Manchester code	Rmch		64		

Handling Procedures

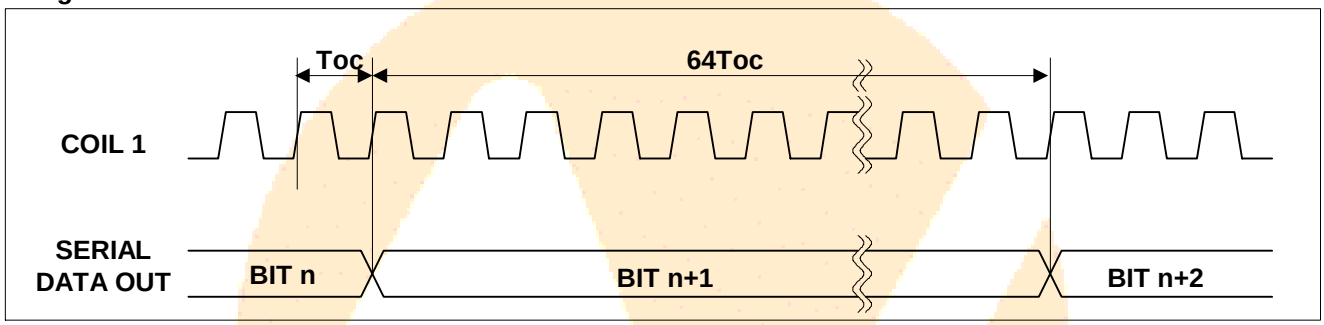
This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component.

Unless othewise specified proper operation can only occur when all terminal voltages are kept within the supply voltage range.

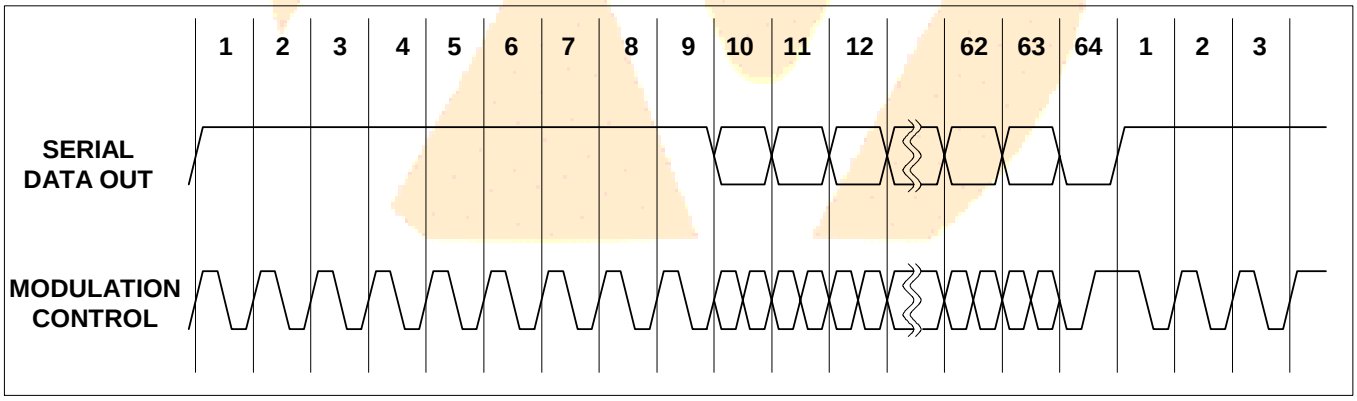
Unused inputs must always be tied to a defined logic voltage level.

Stresses above mentioned maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

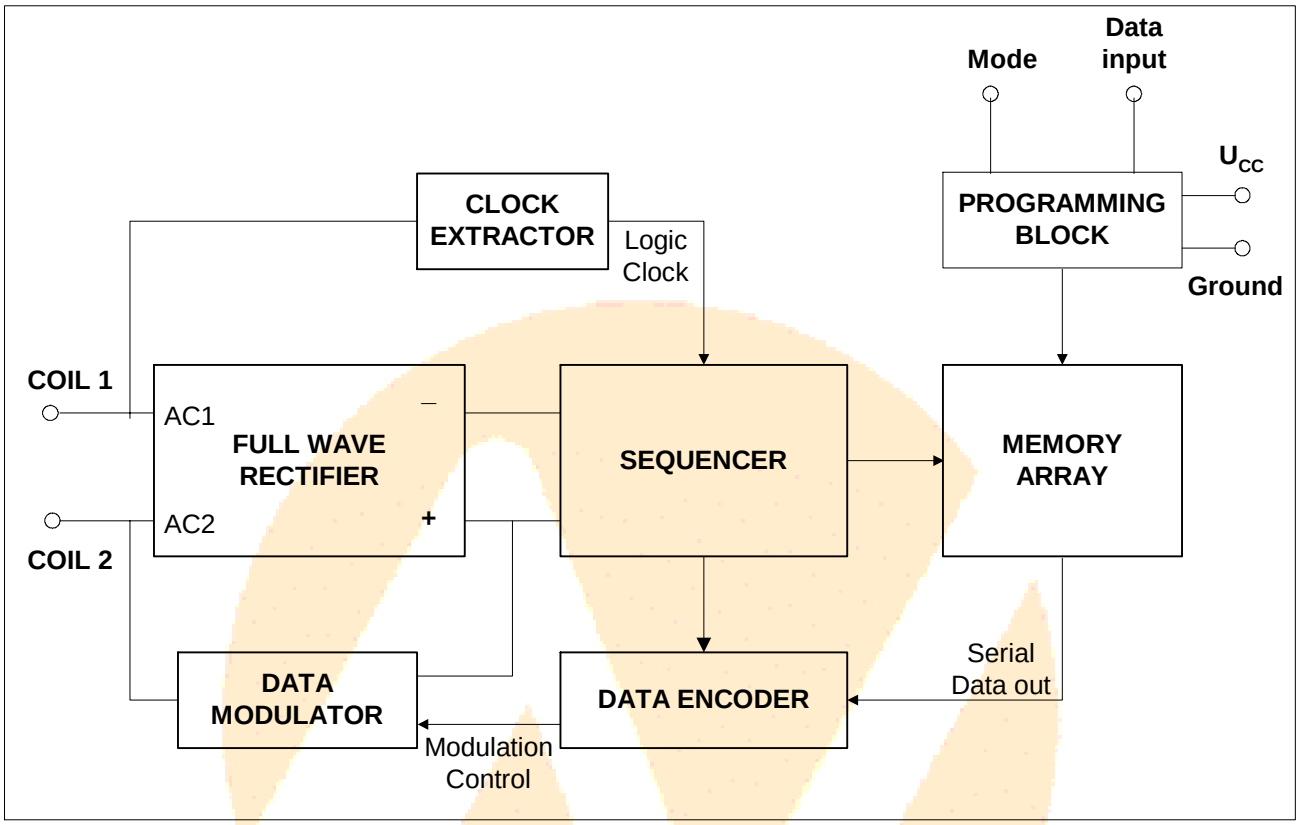
Timing Waveform



Manchester coded waveform



Block Diagram



Functional Description

Full Wave Rectifier

The AC input induced in the external coil by an incident magnetic field is rectified by a Grates bridge

Memory Array

The NT8805C contains 64 bits divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0 ~ P9), 4 column parity bits (PC0 ~ PC3), 40 data bits (D00 ~ D93), and 1 stop bit set to logic 0.

1	1	1	1	1	1	1	1	1	9 Bits Header
8 Version bits or Customer ID				D00	D01	D02	D03	P0	4 data bits & associated even row parity bit
				D10	D11	D12	D13	P1	
				D20	D21	D22	D23	P2	
				D30	D31	D32	D33	P3	
32 Data Bits allowing 4 billion of combinations				D40	D41	D42	D43	P4	
				D50	D51	D52	D53	P5	
				D60	D61	D62	D63	P6	
				D70	D71	D72	D73	P7	
				D80	D81	D82	D83	P8	
				D90	D91	D92	D93	P9	
				PC0	PC1	PC2	PC3	0	4 column even parity bits, NO row parity bit

The header is composed of the 9 first bits which are mask programmed to 111111111. Due to the data and parity organization, this sequence can not be reproduced in the data string. The header is followed by 10 groups of 4 data bits and 1 even row parity bit. Then, the last group consists of 4 even column parity bits.

Bits D00 to D03 and bits D10 to D13 are customer specific identification.

These 64 bits are output serially in order to control the modulator used to modify the current at one of the coil terminals.
When the 64 bits data string is output, the output sequence is repeated continuously until power goes off.

Control Logic

Control logic will modulate the amplitude of the magnetic field with a bit rate corresponding to 64 periods of the field frequency (Manchester coding).
One of the coil terminals (COIL1 in Block Diagram) is used to generate the clock signal for the logic. The output of the clock extractor drives a sequencer providing all necessary signals to address the Memory Array, and serially output the data.

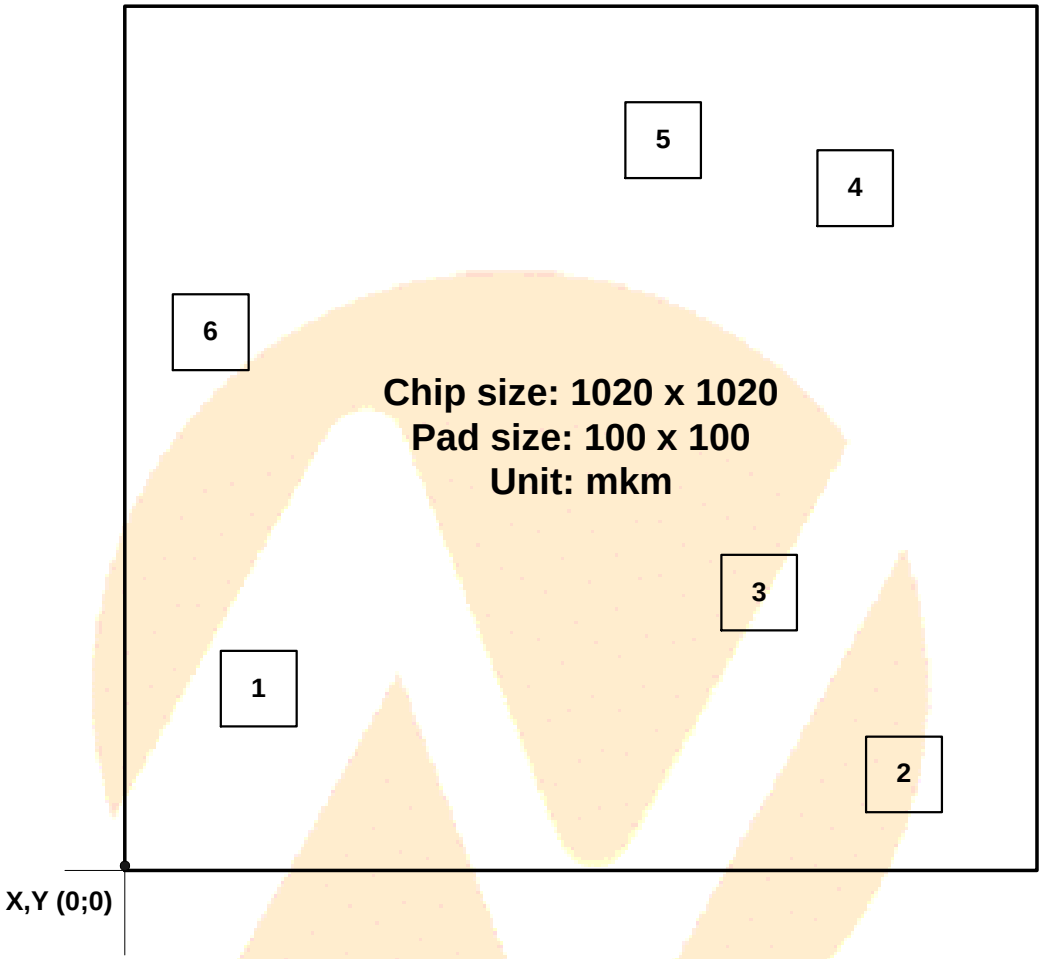
Data Modulator

The Data Modulator is controlled by the Modulation Control signal to induce high current at the Coil 2 terminal when this signal is at logic 0. This will affect the magnetic field in accordance with the data stored in the Memory Array.

Programming Block

When the MODE input is at logic 1 level every two clock pulses on Coil 1 cause serial data shift in the Memory Array. A high voltage (> 10V) level at the DATA input results in polysilicon fuse blowing.

PAD DIAGRAM



NOTE:
*Resonance loop is connected between COIL1 (pad 1) and COIL2 (pad 3)
*The rest of the pads are not used when bonding.

PAD LOCATION

Pad number	Pad name	X	Y	Pad number	Pad name	X	Y
1	COIL	120.7	120.3	4	COIL	912.5	912.1
2	Programming input (Pr)	939.3	69.3	5	U_{CC}	694.0	937.6
3	GND	727.2	337.5	6	Data input (Dir)	84.2	762.5